AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor storage apparatus to be coupled with a system bus to receive a write request accompanied with first and second sectors of data, comprising~~:~~

a plurality of nonvolatile semiconductor memories which store said first and second sectors of data therein; and

a control module to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control module refers to a table for selecting ~~an arbitrary one or more~~ a first one of said nonvolatile semiconductor memories and sends a first erase command to said first one of said ~~plurality of~~ nonvolatile semiconductor memories to initiate a first internal erase operation of data within said first one of said ~~plurality of~~ nonvolatile semiconductor memories, ~~and~~

wherein, after said first erase command has been sent, said control module sends a second erase command to ~~another~~ a second of said ~~plurality of~~ nonvolatile semiconductor memories, different from said first one of said ~~plurality of~~ nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data within said second ~~other~~ of said ~~plurality of~~ nonvolatile semiconductor memories while said first one of said ~~plurality of~~

nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command,

wherein said control module updates a designation of the nonvolatile semiconductor memories in the table after each occurrence of sending an erase command to a respective nonvolatile semiconductor memory, and

wherein said control module executes status polling from the first nonvolatile semiconductor memory to which said first erase command has been sent and is followed by executing status polling from the second~~other~~ nonvolatile semiconductor memory to which said second erase command has been sent.

2. (Currently Amended) A semiconductor storage apparatus according to claim 1, ~~farther~~ further comprising:

a buffer memory, coupled commonly with said plurality of nonvolatile semiconductor memories, which holds said first and second sectors of data as write data to be written into said plurality of nonvolatile semiconductor memories,

wherein said control module responds to said write request, carries out read operations of said first and second sectors of data as said write data from said buffer memory and carries out write operations of said first and second sectors of data as said write data read out from said buffer memory into said plurality of nonvolatile semiconductor memories, wherein said write operations into said plurality of nonvolatile semiconductor memories are controlled by sending a first write command from said control module to one of said plurality of nonvolatile semiconductor memories and by sending a second write command from said control module to another of said plurality of nonvolatile semiconductor memories, different from said one to which said first write command has been sent, while said one of said plurality

of nonvolatile semiconductor memories is still performing a write operation responsive to said first write command.

3. (Original) A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

4. (Original) A semiconductor storage apparatus according to claim 2, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

5. (Original) A semiconductor storage apparatus according to claim 2, wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

6. (Previously Presented) A semiconductor storage apparatus according to claim 1, wherein said control module includes a processor.

7. (Previously Presented) A semiconductor storage apparatus according to claim 2, wherein said control module includes a processor

8. (Previously Presented) A semiconductor storage apparatus according to claim 1, wherein said control module further includes an address controller.

9. (Previously Presented) A semiconductor storage apparatus according to claim 2, wherein said control module further includes an address controller,

10. (Original) A semiconductor storage apparatus according to claim 1,

wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and

wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

11. (Original) A semiconductor storage apparatus according to claim 2,

wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and

wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 byte which is a sector capacity of a standard disk.

12. (Previously Presented) A semiconductor storage apparatus according to claim 10, wherein said control module includes a processor.

13. (Previously Presented) A semiconductor storage apparatus according to claim 11, wherein said control module includes a processor.

14. (Previously Presented) A semiconductor storage apparatus according to claim 10, wherein said control module further includes an address controller.

15. (Previously Presented) A semiconductor storage apparatus according to claim 11, wherein said control module further includes an address controller.

16. (Currently Amended) A semiconductor storage apparatus to be coupled with a system bus comprising:

a plurality of nonvolatile semiconductor memories which write data from said system therein in sector units and erase said data in block units, ~~said~~ each block including a plurality of said sectors; and

a control module to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control module refers to a table for selecting ~~an arbitrary one or more~~a first one of said nonvolatile semiconductor memories and sends a first erase command to said first one of said ~~plurality of~~ nonvolatile semiconductor memories to initiate a first internal erase operation of data in said block units within said first one of said ~~plurality of~~ nonvolatile semiconductor memories, ~~and~~

wherein, after said first erase command has been sent, said control module sends a second erase command to ~~an other~~ a second of said ~~plurality of~~ nonvolatile semiconductor memories, different from said first one of said ~~plurality of~~ nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data in said block units within said ~~other~~ second of said ~~plurality of~~ nonvolatile semiconductor memories while said first one of said ~~plurality of~~ nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command.

wherein said control module updates a designation of the nonvolatile semiconductor memories in the table after each occurrence of sending an erase command to a respective nonvolatile semiconductor memory, and

wherein said control module executes status polling from the first nonvolatile semiconductor memory to which said first erase command has been sent and is followed by executing status polling from the second nonvolatile semiconductor memory to which said second erase command has been sent.

17. (Cancelled)

18. (New) A semiconductor storage apparatus according to claim 1, wherein the status polling comprises determining whether a predetermined signal has a predetermined value.

19. (New) A semiconductor storage apparatus according to claim 18, wherein the predetermined signal comprises one data bit of a plurality of data bits.

20. (New) A semiconductor storage apparatus according to claim 16, wherein the status polling comprises determining whether a predetermined signal has a predetermined value.

21. (New) A semiconductor storage apparatus according to claim 20, wherein the predetermined signal comprises one data bit of a plurality of data bits.